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COMPARATIVE ANALYSIS OF MODULATION TECHNIQUES FOR CHB MULTILEVEL INVERTERS

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Abstract - A multilevel inverter (MLI) is a power electronic device that is used for high-power and high-voltage applications and has many advantages like reduced total harmonic distortion (THD) and high-power quality waveform. Hence, the size and bulkiness of passive filters can be reduced. The output voltage of the multi-level inverter is in a staircase waveform. Therefore, the voltage stress of the switching device is lower, and the total harmonic distortion (THD) is also lower than that of the other types of inverters. As the number of DC voltage sources increases in input side, the sinusoidal like waveform can be generated at the output of inverter. In this paper, a CHB 7-level inverter is discussed using two modulation techniques. In the present work, the Sinusoidal Pulse Width Modulation (SPWM) and nearest level control (NLC) method are used. The SPWM scheme provides the best harmonic profile in high frequency switching. The nearest level control method is used in low switching frequency, which leads to reduction of switching losses. The model is simulated using SPWM and nearest level modulation techniques and the effect of the harmonic spectrum is analyzed.

Keywords: Cascaded H-bridge, 7-Level Inverter, Nearest Level Control, Sinusoidal PWM.

1. INTRODUCTION

The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as inverter. [1] Multilevel inverters are used for high power and high voltage applications and have many advantages like high power quality waveform, reduced total harmonic distortion (THD). [2] Hence, the size and bulkiness of passive filters can be reduced. These inverters generate a stepped voltage waveform by proper arrangement of semiconductor devices and number of dc voltage sources as an input. [3]

The multilevel inverters are primarily classified as Flying capacitor inverter, Diode clamped and Cascaded H–Bridge multilevel inverter. [4] Cascaded H–Bridge (CHB) multilevel inverter needs a number of isolated dc supplies, each of which feeds an individual H-bridge power cell. [5] The number of H-bridge cells in a CHB inverter is mainly decided by the inverter operating voltage, harmonic requirements, and manufacturing cost. [6] The output voltage of the multi-level inverter is in a staircase waveform.

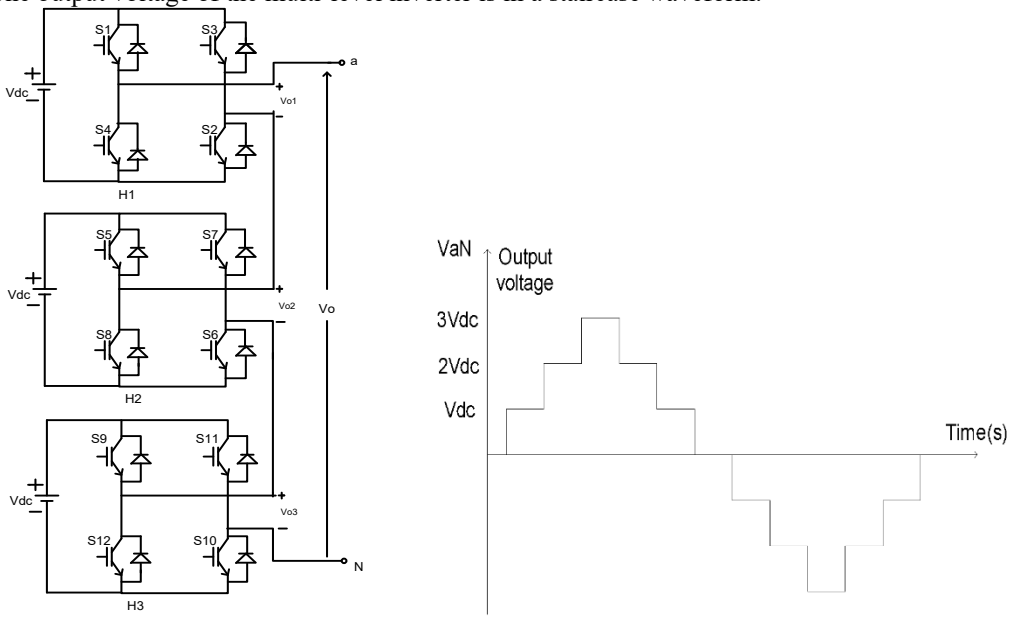

Fig. 1.1 Per Phase Diagram of Conventional CHB 7-level Inverter

Therefore, the voltage stress of the switching device is lower, and the total harmonic distortion (THD) is also lower than that of the other types of inverters [7]. As the number of DC voltage sources increases in input side, the sinusoidal like waveform can be generated at the output of inverter [8]. Increasing the number of levels of the multi-level inverter (MLI) provides more steps for approximating the desired output waveform and reduced

harmonic distortion and dv/dt stress [9]
Conventional cascaded multilevel inverter consists of a number of single-phase H-bridge inverters. The CHB inverter with seven to eleven voltage levels has been widely used in high-power and medium-voltage applications. [10] IGBTs are exclusively used as switching devices in these inverters.
A stepped output voltage and current can be obtained in a cascaded multilevel inverter by cascading many H-bridge inverters. In conventional CHB7-level Inverter, three H-bridge inverters are to be cascaded to get a 7-level output. [11]
From figure 1, when switches S1, S2, S5, S6, S9, S10 conduct, the output voltage of the H-bridge cells H1, H2 and H3 is Vo1=Vo2=Vo3=Vdc and the resultant inverter phase voltage is VaN=Vo=Vo1+Vo2+Vo3= 3Vdc, which is the voltage at the inverter terminal 'a' with respect to the inverter neutral N. Similarly, with S3, S4, S7, S8, S11, S12 switched on, VaN = –3Vdc. The other five voltage levels are 2Vdc, Vdc, 0, -Vdc, -2Vdc which correspond to various switching states given in table 1 [12].

Table-1.1 Seven- level CHB Inverter (Single Phase) Switching States and Corresponding Output Voltages

State	Device Switching States												Inverter Terminal Voltage (VaN)
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	
1	1	1	0	0	0	1	0	1	0	1	0	1	**+Vdc**
2	1	1	0	0	1	1	0	0	0	1	0	1	**+2Vdc**
3	1	1	0	0	1	1	0	0	1	1	0	0	**+3Vdc**
4	1	0	1	0	1	0	1	0	1	0	1	0	**0**
	0	1	0	1	0	1	0	1	0	1	0	1	
5	0	0	1	1	0	1	0	1	0	1	0	1	**-Vdc**
6	0	0	1	1	0	0	1	1	0	1	0	1	**-2Vdc**
7	0	0	1	1	0	0	1	1	0	0	1	1	**-3Vdc**

2. METHODOLOGY

The nearest level control technique is used in the proposed work for the pulse generation for both 12 switch and 6 switch inverter configurations. This control method tends to generate a staircase voltage which minimizes the error with respect to the reference voltage and is known as nearest level (or round) control method [13]. In this method, the sinusoidal reference voltage is compared with the available dc voltage levels and the level is chosen that is nearest to the reference voltage [14]. Consequently, the proper switches are turned on to generate the desired voltage level. The output voltage (vo) will be staircase voltage with minimum possible error with respect to the reference voltage. The circuits are modeled and simulated using MATLAB/Simulink.
Level shifting scheme is further divided into three schemes - Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternate Phase Opposition Disposition (APOD). Phase disposition involves all the carriers that are in phase. All the carrier waves above zero reference are in phase while the ones below zero are 180 degrees out of phase in case of phase opposition disposition. Each carrier is 180 degrees in phase difference with its neighboring carrier in alternate phase opposition disposition [15]. While using level shifting scheme, an 'm' level inverter requires 'm-1' triangular carrier waves, all having the same frequency and amplitude. The (m-1) triangular carriers are vertically disposed such that the bands they occupy are contiguous. The frequency modulation index is given by mf = fc/fm, where fm is modulating frequency and fc is carrier waves frequency. Whereas the amplitude modulation index is defined as ma=Vm/Vc(m-1), for $0 \leq m_a \leq 1$ Where Vm is the peak value of the modulating wave and V_c is the peak value of each carrier wave. For seven-level inverter, using SPWM technique, six carrier waveforms are arranged so that every carrier is in phase. Three of them are applied across the positive half cycle of the modulating signal, remaining three of them are applied across the negative half cycle of the modulating signal. From these signals twelve PWM signals are generated and then given to the twelve switches of a leg. [16]

3. SIMULATION RESULTS

The power circuit and control circuit of seven-level inverter is simulated using carrier based PWM technique, i.e. SPWM technique and fundamental frequency control method i.e. nearest level control (NLC) method. Harmonic spectrum analysis is done using FFT window using MATLAB/Simulink.
Figure 3.1 shows simulation model of one phase-leg of a seven-level CHB inverter. As shown in figure 2, when switches S1, S2, S5, S6, S9, S10 conduct, the output voltage of the H-bridge cells *H1, H2 and H3* is

Vo1=Vo2=Vo3= Vdc and the resultant inverter output voltage is VaN=Vo=Vo1+Vo2+Vo3 = 3Vdc, which is the voltage at the inverter terminal a with respect to the inverter neutral *N*. Similarly, with S3, S4, S7, S8, S11, S12 switched on, VaN = –3Vdc. Switching Pattern Produced using SPWM scheme is shown in figure 3.1.

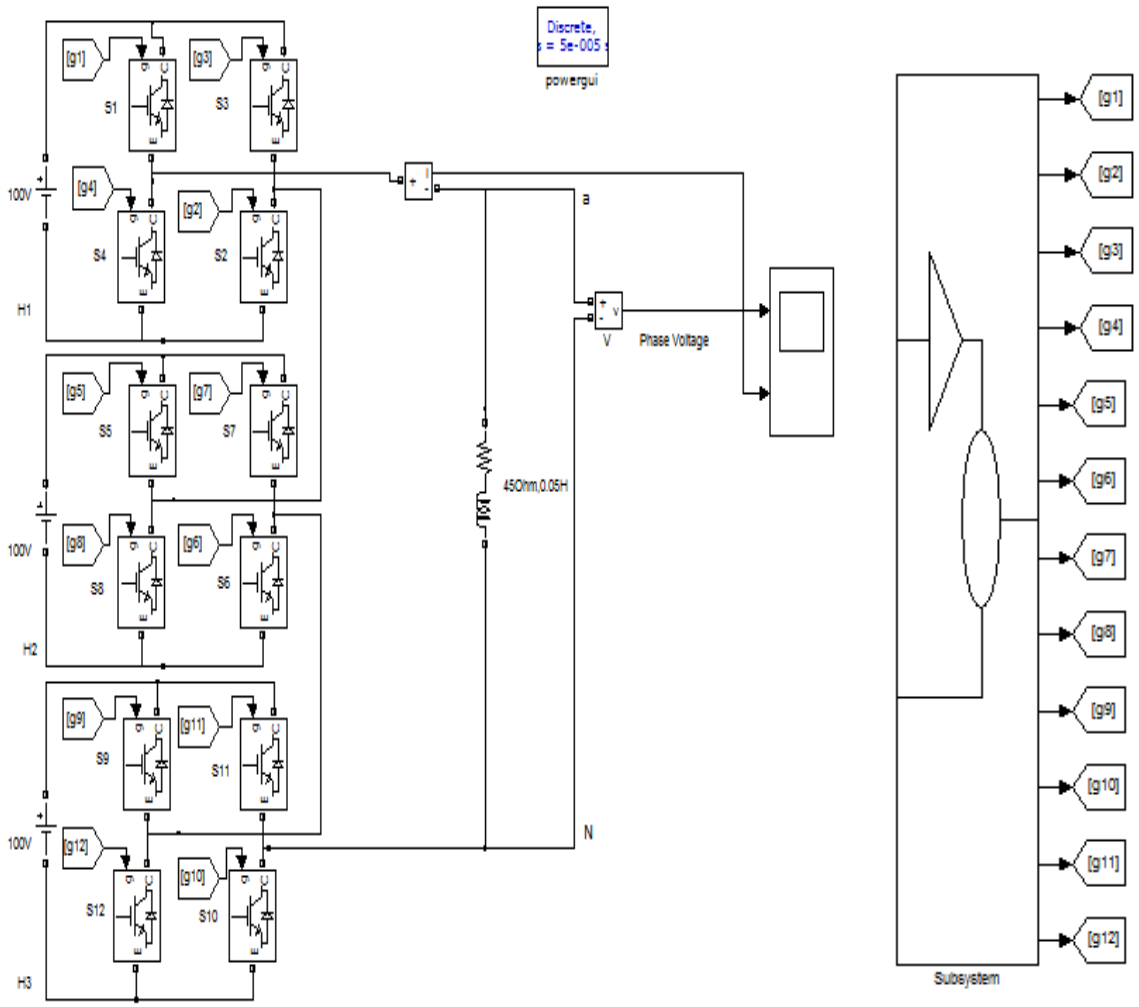

Fig. 3.1 Simulation Model of Seven-level CHB Inverter (Single Phase)

Table-3.1 Simulation Parameters for Seven- level CHB Inverter

DC Bus Voltage (Vdc)	100 V
Carrier frequency	2.250 KHz
Fundamental frequency	50Hz
Control technique	SPWM
Load	R=45 Ohm, L=0.05H

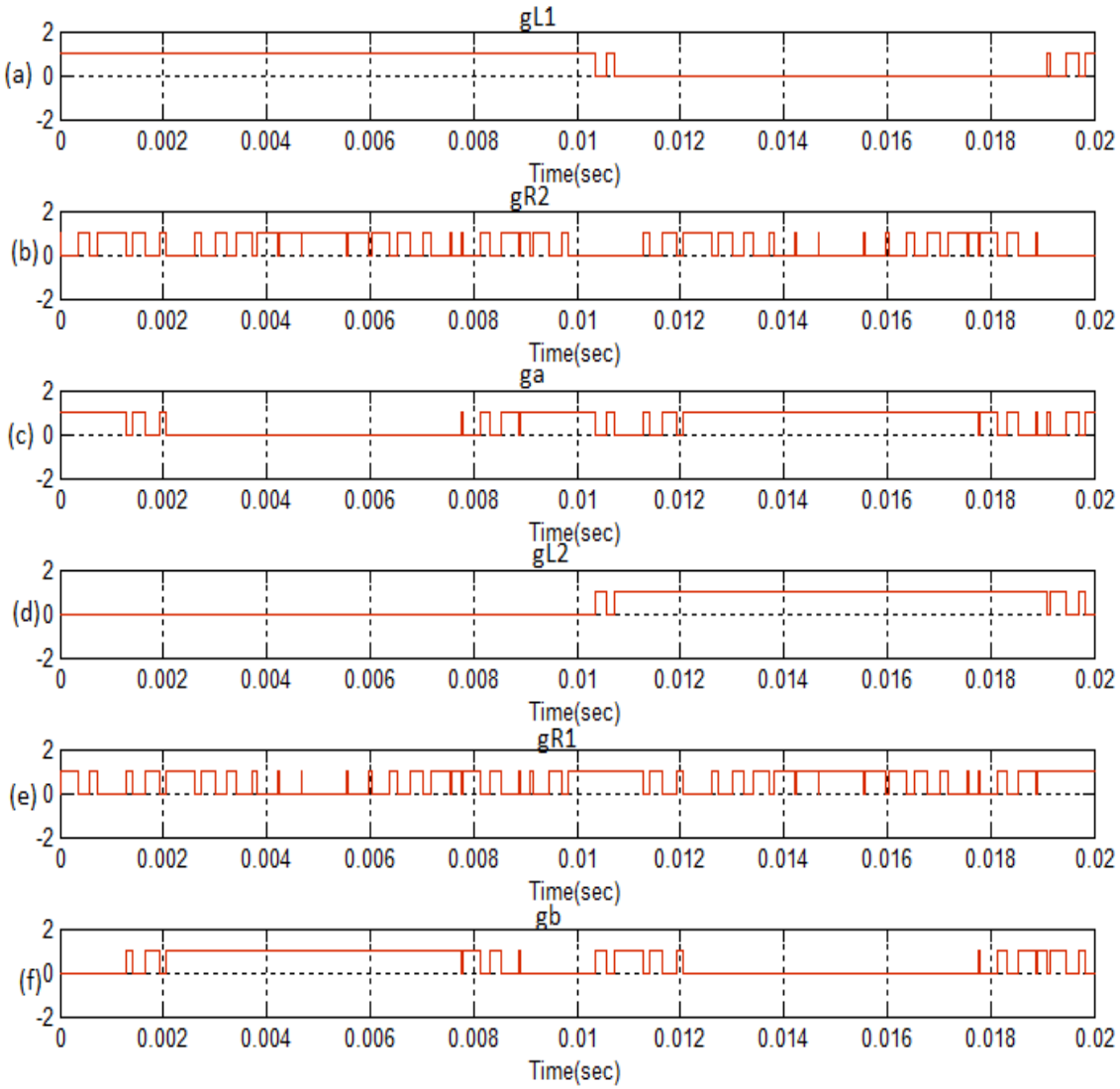

Fig. 3.2 Switching Pattern Produced using SPWM scheme

Simulation results of One Phase Leg of Seven-level CHB Inverter using SPWM technique with modulation index (ma) of 1 are as given below:

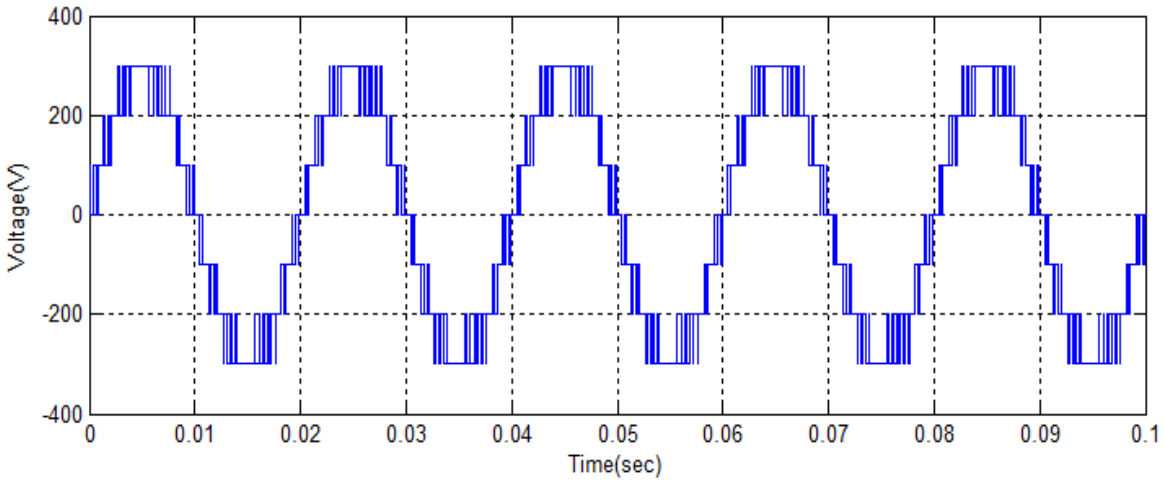

Fig. 3.3 Output Phase Voltage Waveform of Seven-level CHB Inverter using SPWM

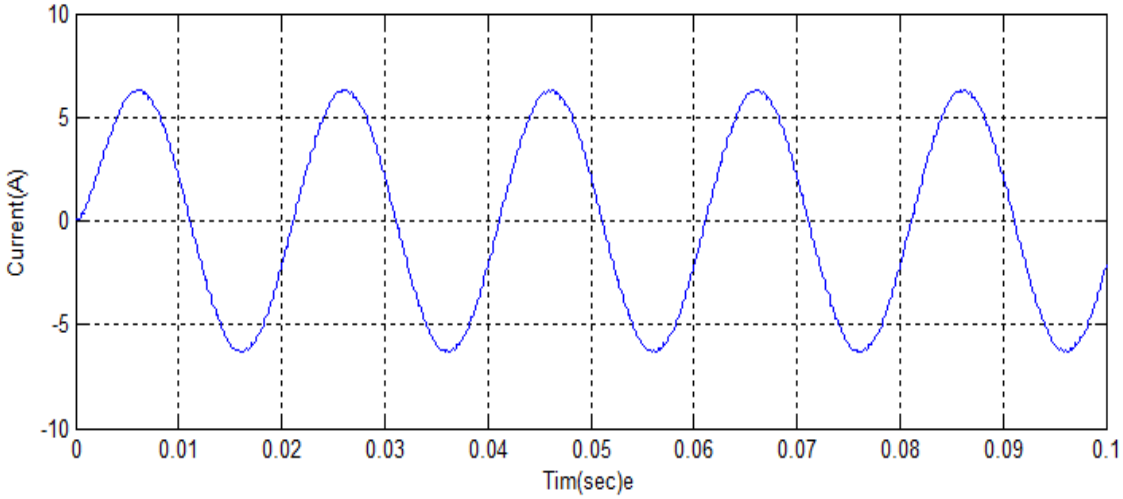

Fig. 3.4 Output Phase Current Waveform of Seven-level CHB Inverter using SPWM

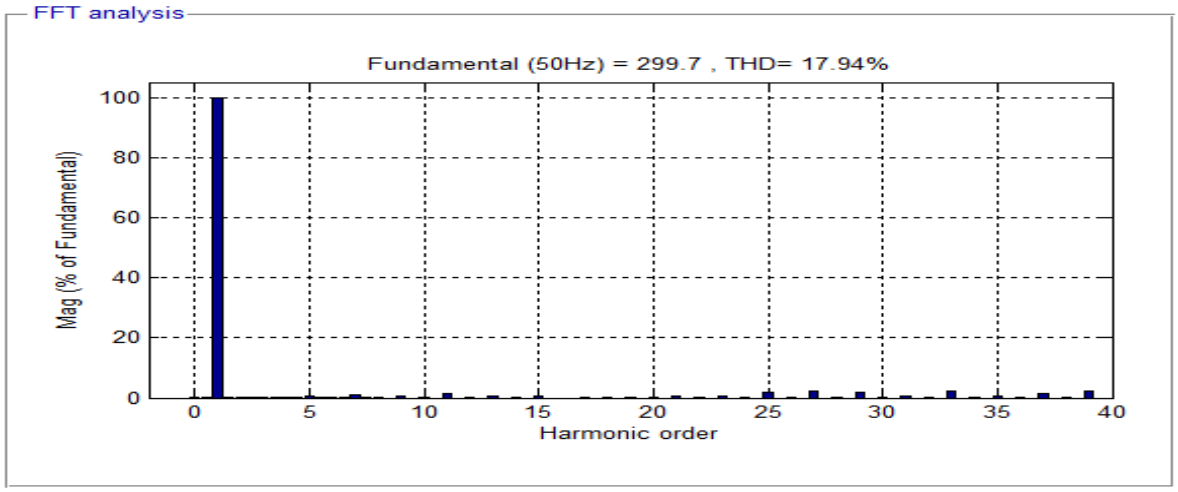

Fig. 3.5 FFT Analysis of Seven-level Cascaded H-bridge Inverter using SPWM Technique with ma=1

Simulation study of seven-level CHB Inverter using SPWM technique has been carried out. Figure 3.3 shows the output phase voltage waveform and figure 3.4 represents the output current waveform of seven-level CHB inverter. From figure 3.5, which represents the harmonic spectrum for output phase voltage and output current, it is observed that the total harmonic distortion (THD) for the output phase voltage is 17.94%

Simulation results of One Phase Leg of Seven-level CHB Inverter using NLC technique with modulation index (ma) of 1 are as given below:

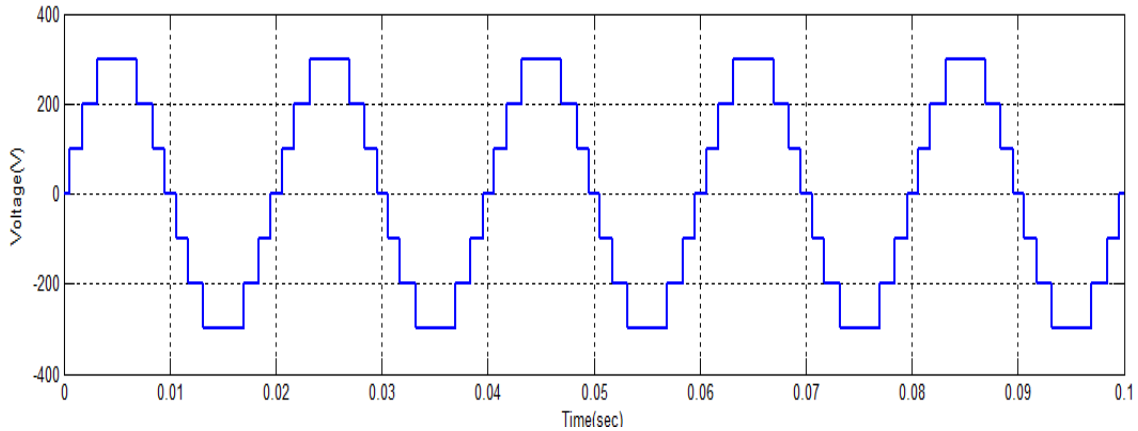

Fig. 3.6 Output Voltage Waveform of Conventional CHB 7-level Inverter using NLC

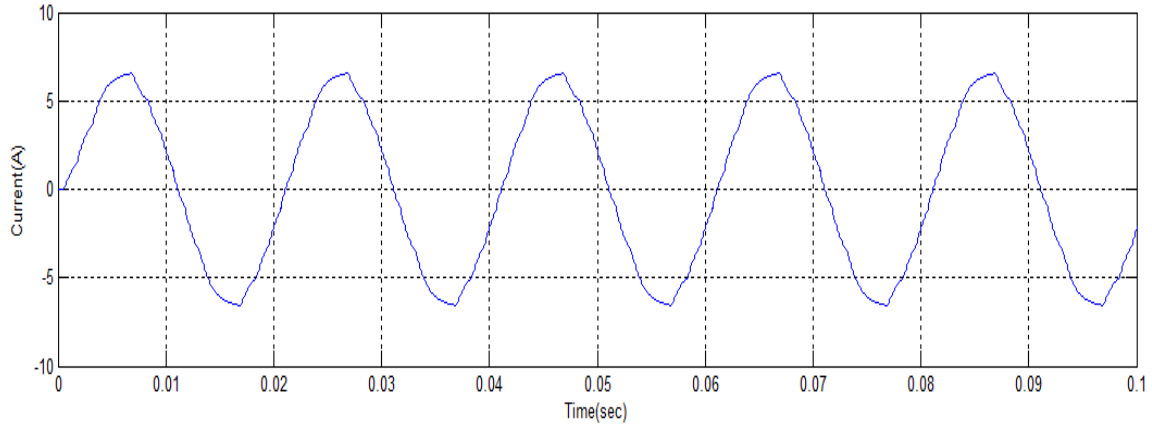

Fig. 3.7 Output Current Waveform of Conventional CHB 7-level Inverter using NLC

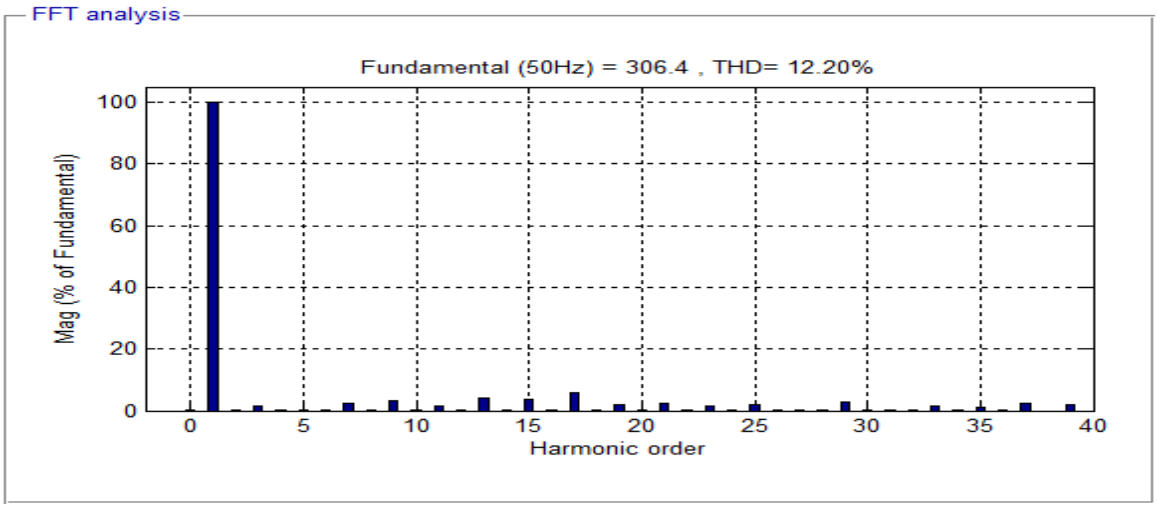

Fig. 3.8 Harmonic Spectrum for Output Phase voltage of Seven-level CHB Inverter using NLC

Simulation study of seven-level CHB Inverter using NLC technique has been carried out. Figure 3.6 shows the output phase voltage waveform and figure 3.7 shows the output current waveform of seven-level CHB inverter. From figure 3.8, which represents the harmonic spectrum for output phase voltage and output current, it is observed that the total harmonic distortion (THD) for the output phase voltage is 12.20%

Table-3.2 Comparison of Two Configurations of 7-Level Inverters

Conventional CHB 7-level inverter	SPWM	NLC
THD	17.94	12.20
Fundamental Voltage(V)	299.7	306.4

CONCLUSION

A comparison of Nearest Level Control (NLC) and Sinusoidal Pulse Width Modulation (SPWM) for a seven-level Cascaded H-Bridge (CHB) inverter shows that both techniques successfully produce high-quality stepped output waveforms. However, simulation results demonstrates that NLC delivers a slightly higher fundamental voltage and achieves a lower total harmonic distortion (THD) of 12.20% compared to 17.94% with SPWM. While NLC is more effective at low switching frequencies because of lower switching losses, SPWM performs better at high switching frequencies. Therefore, the requirements of the particular application should guide the choice of modulation technique, which should balance efficiency, switching frequency, and harmonic performance.

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